

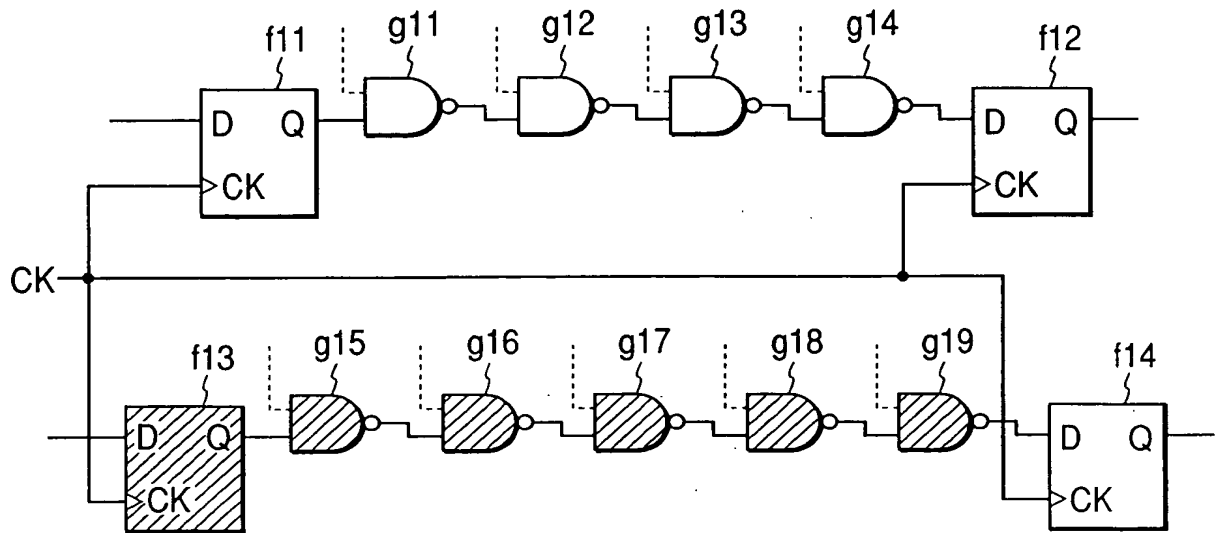
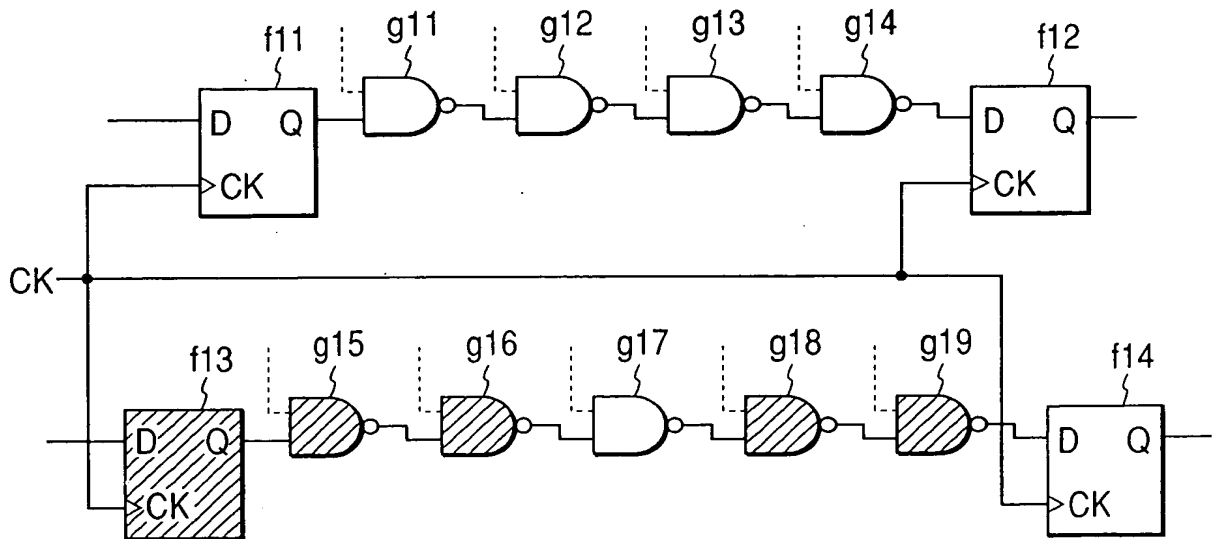
FIG. 1*FIG. 2*

FIG. 3

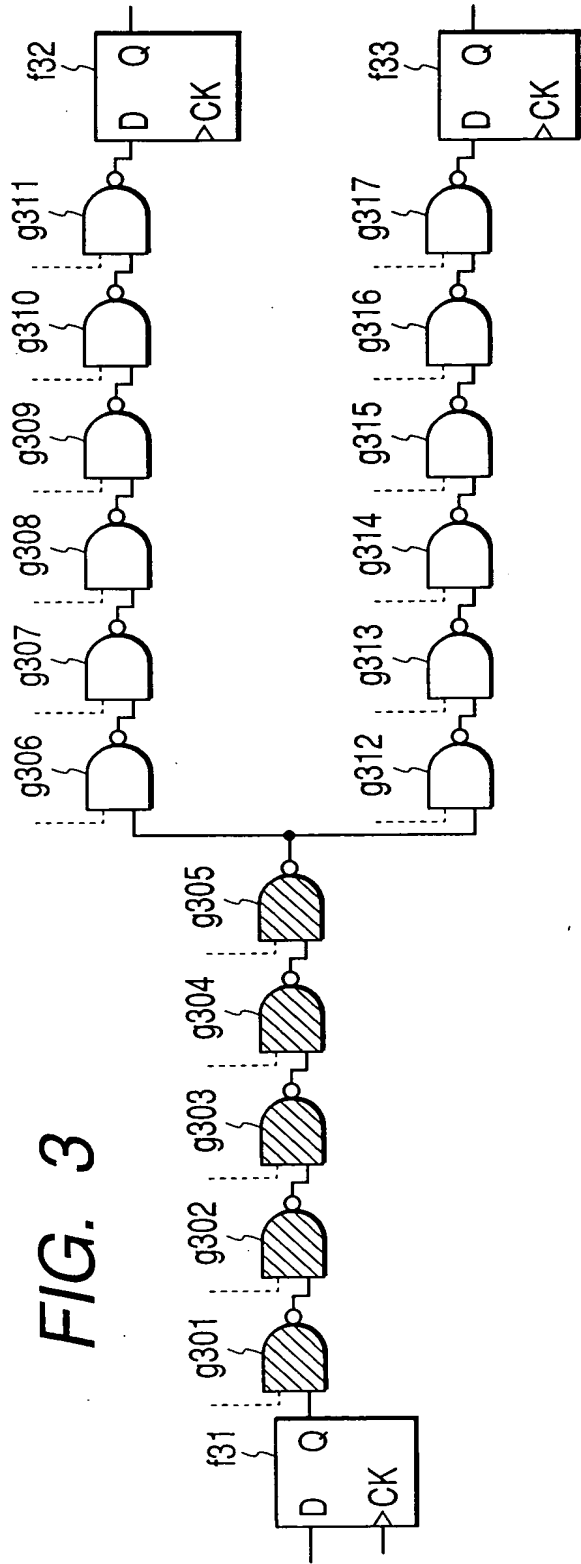


FIG. 4

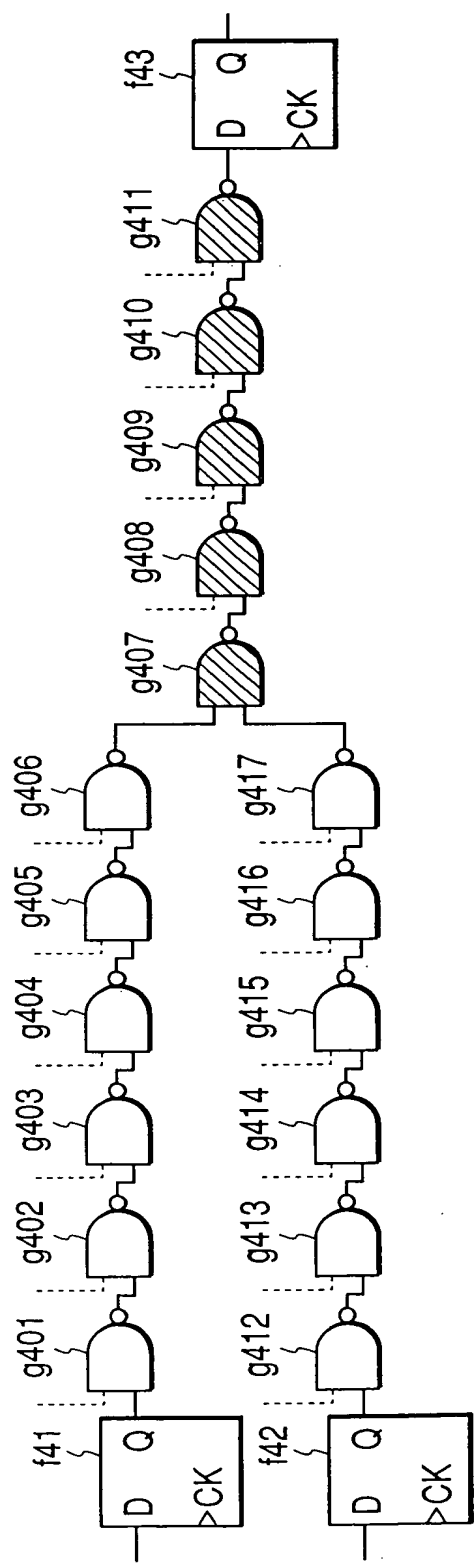


FIG. 5

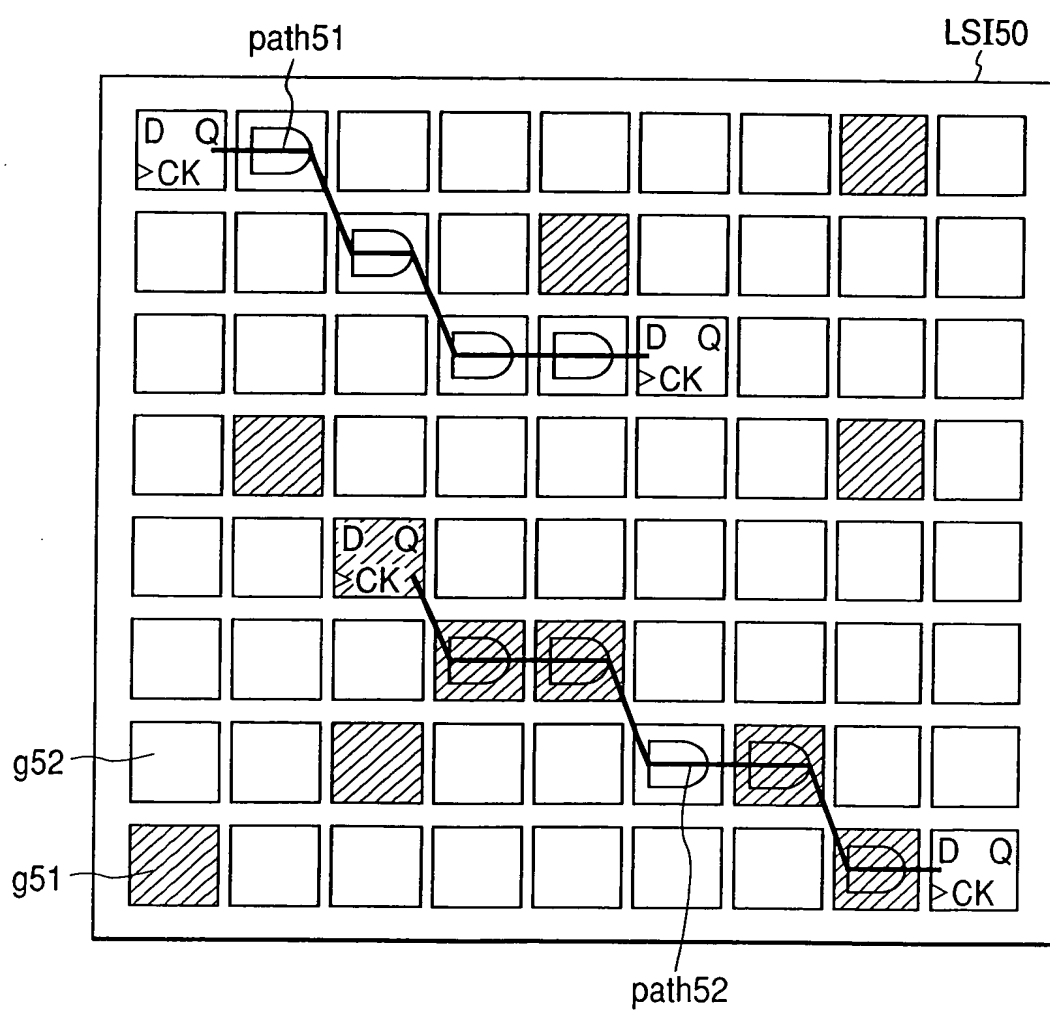


FIG. 6

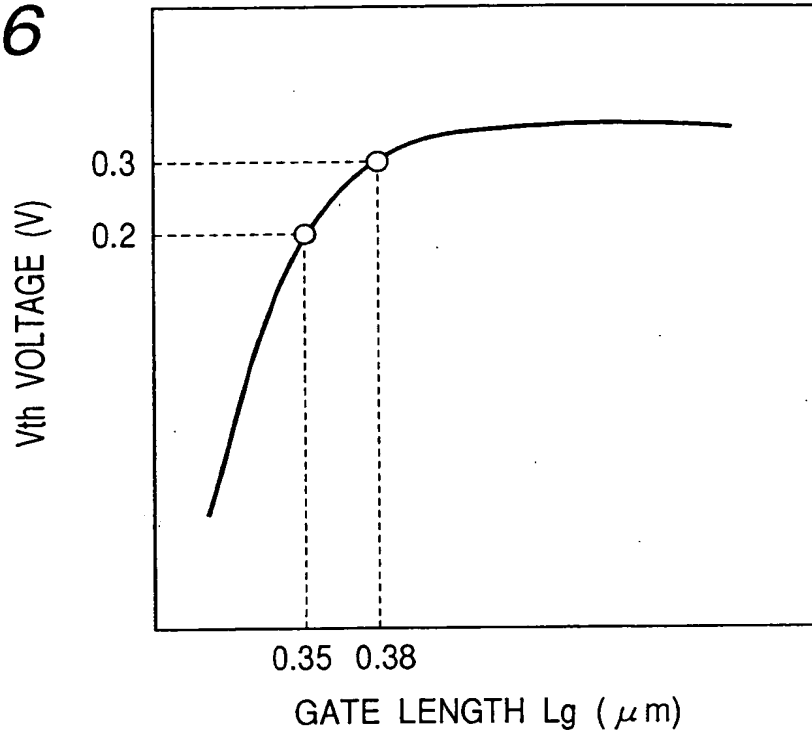


FIG. 7

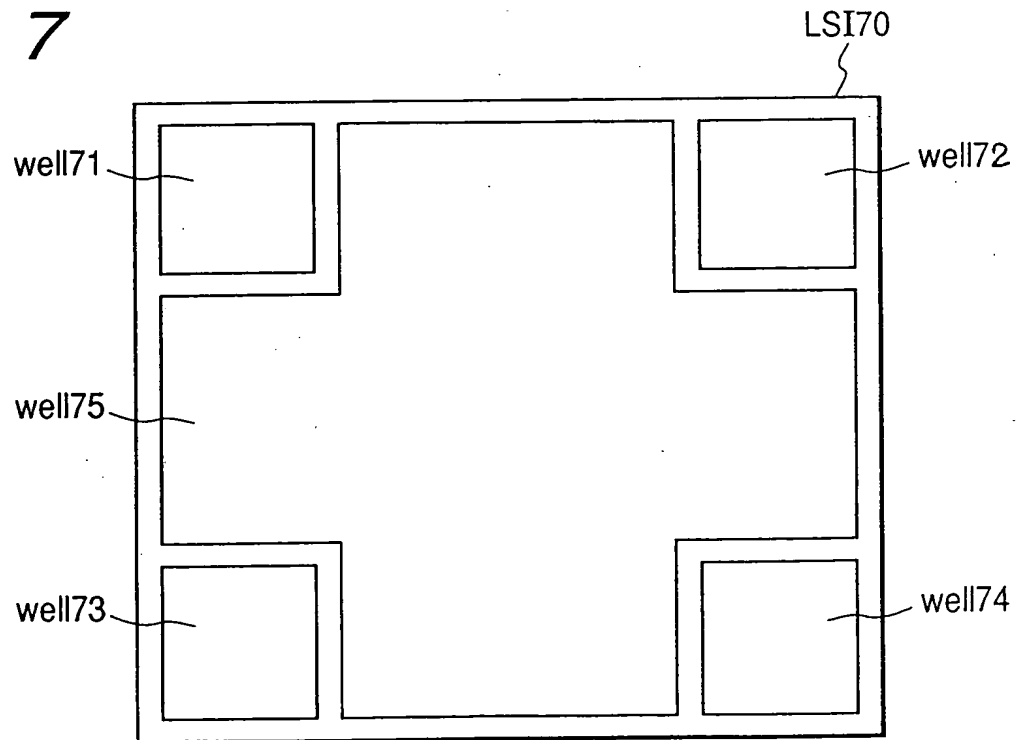


FIG. 8

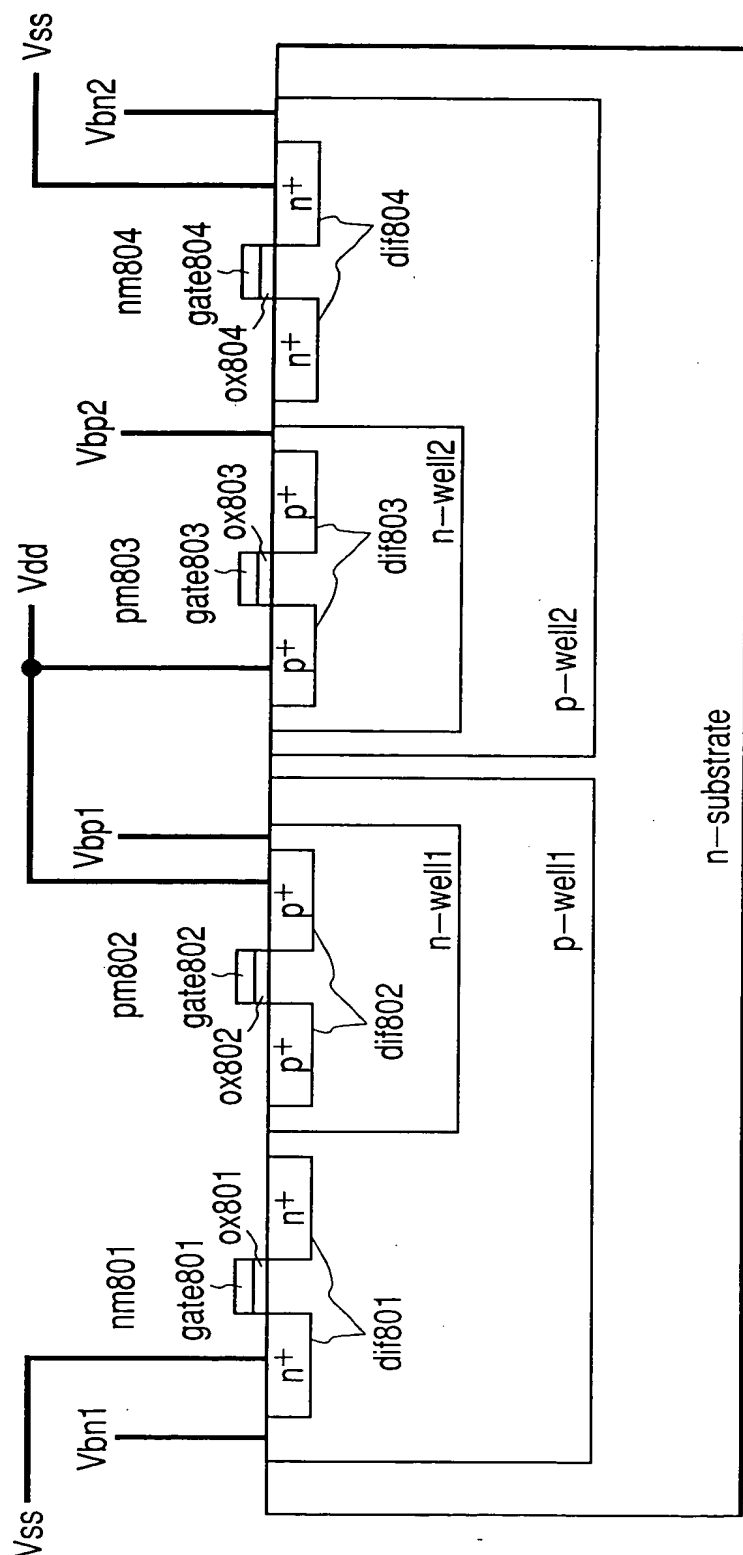


FIG. 9(a)

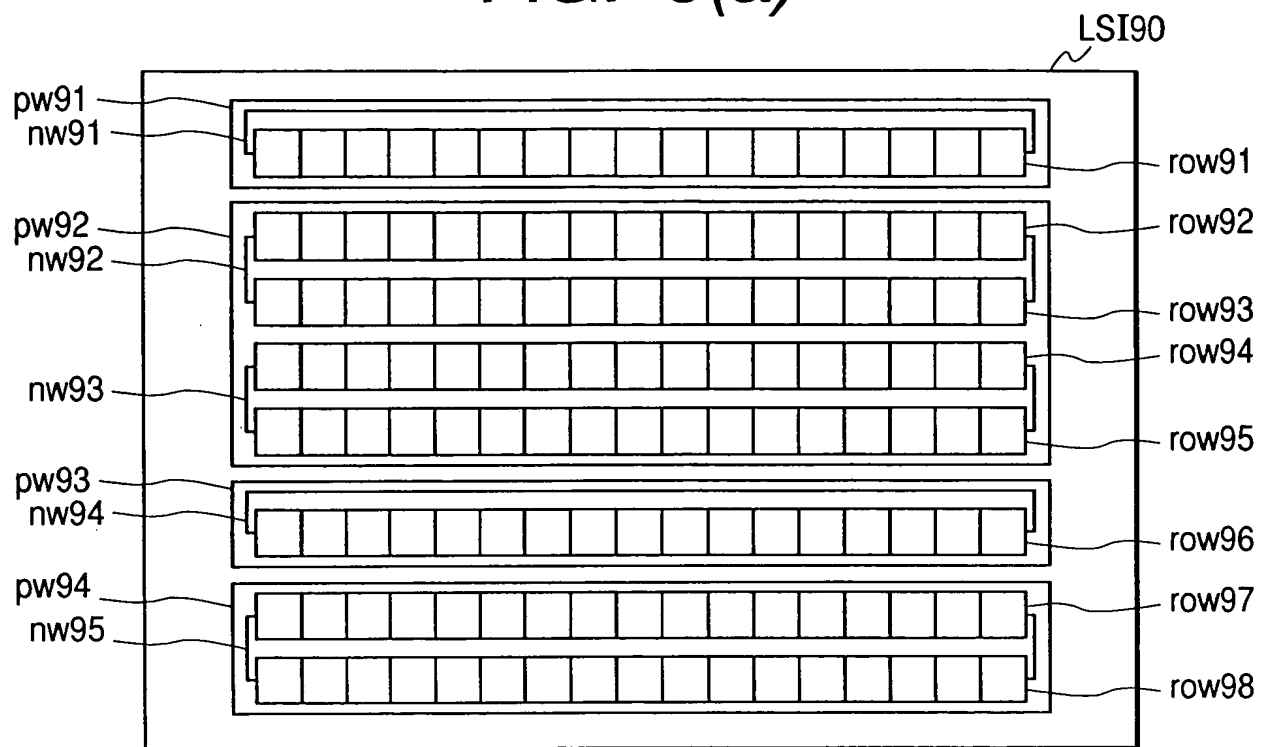


FIG. 9(b)

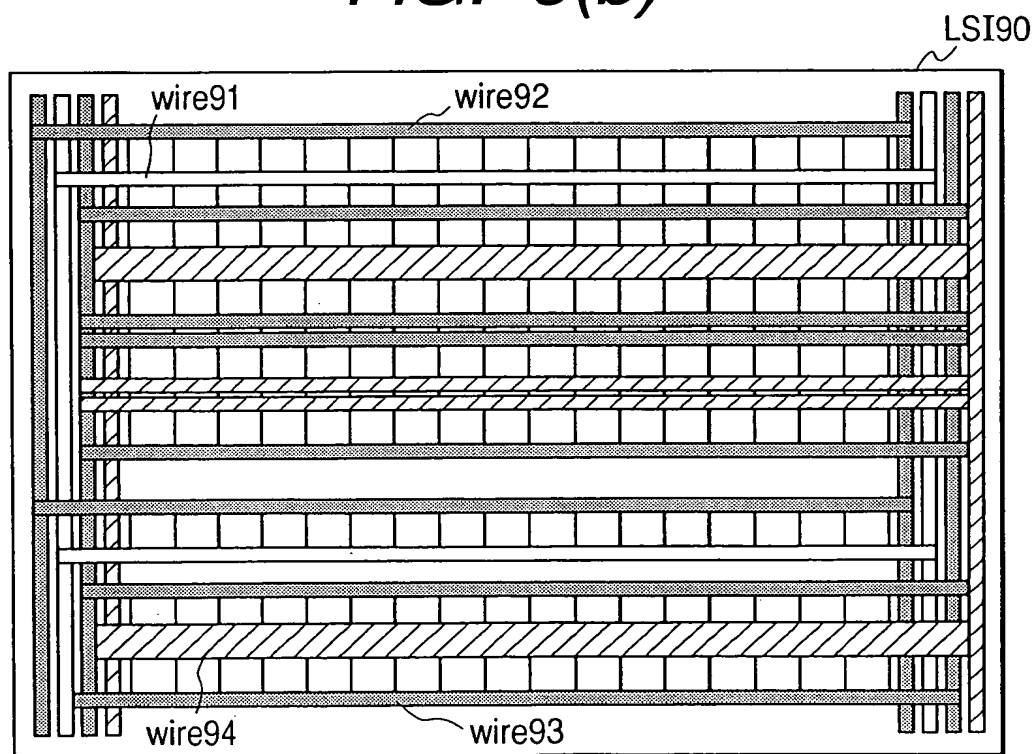


FIG. 10

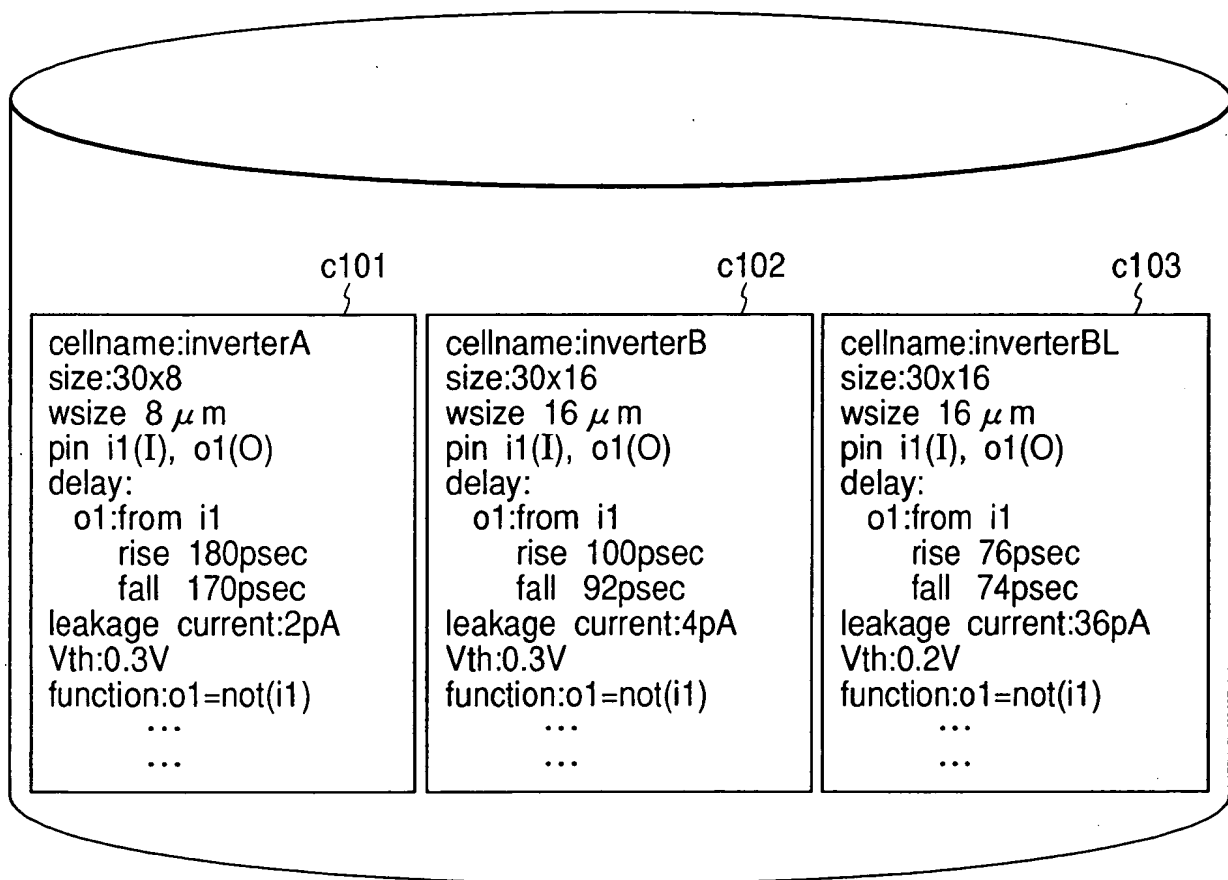


FIG. 11

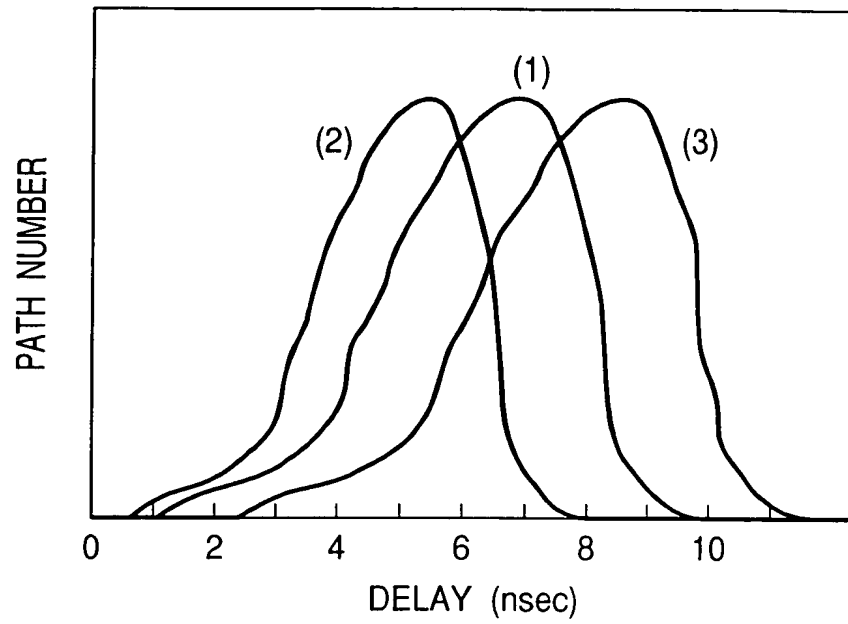
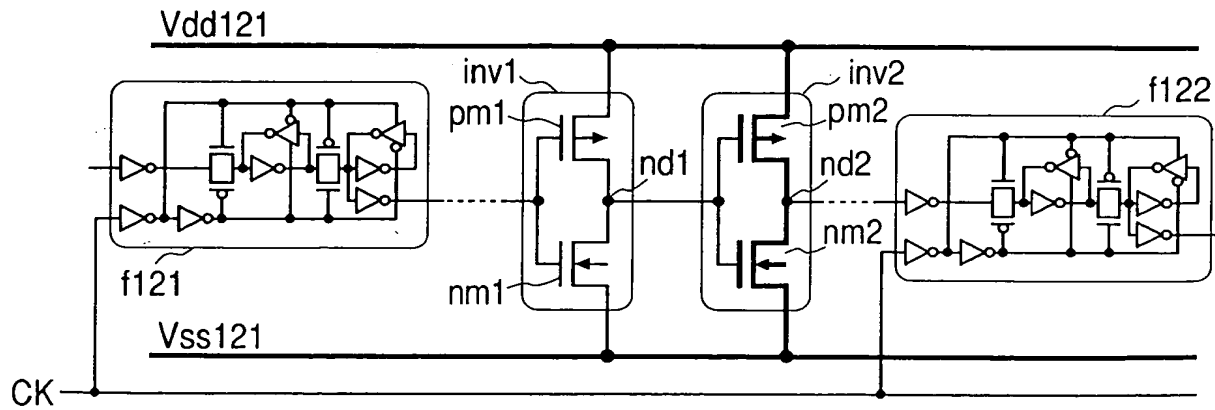


FIG. 12



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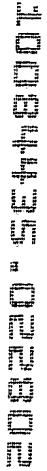


FIG. 14

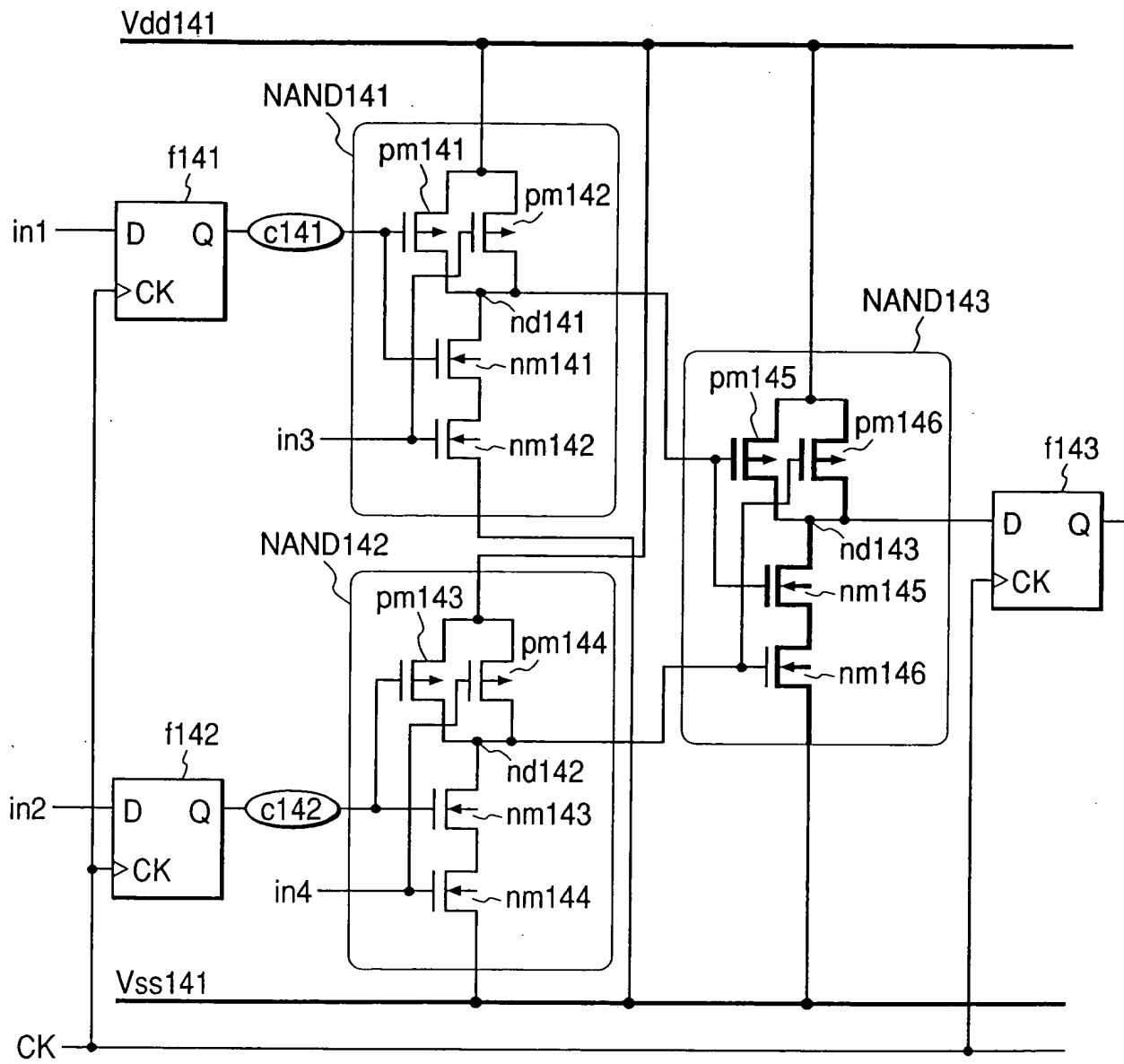


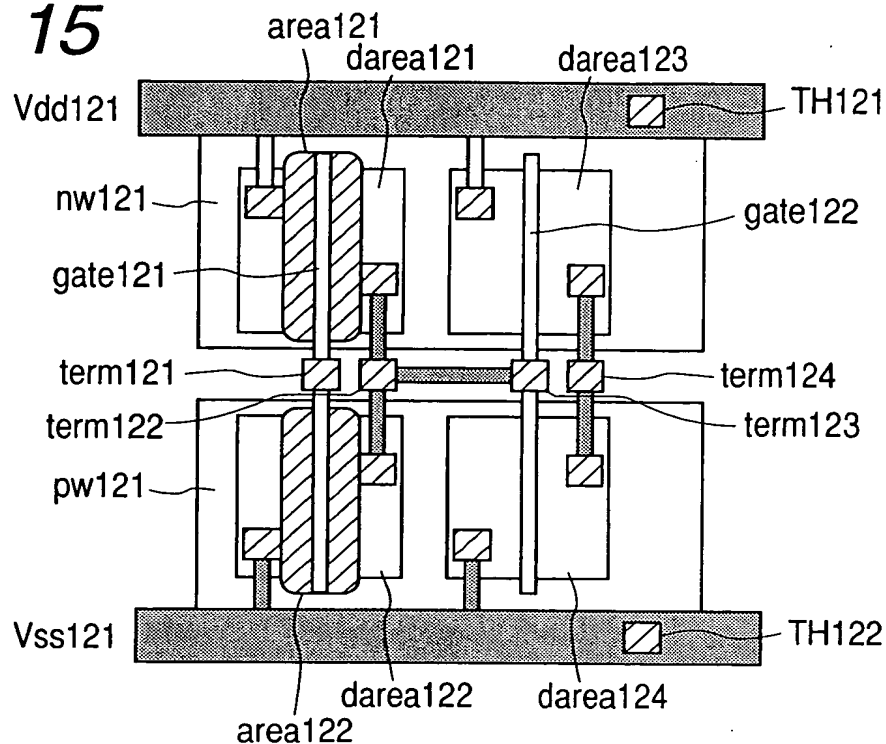
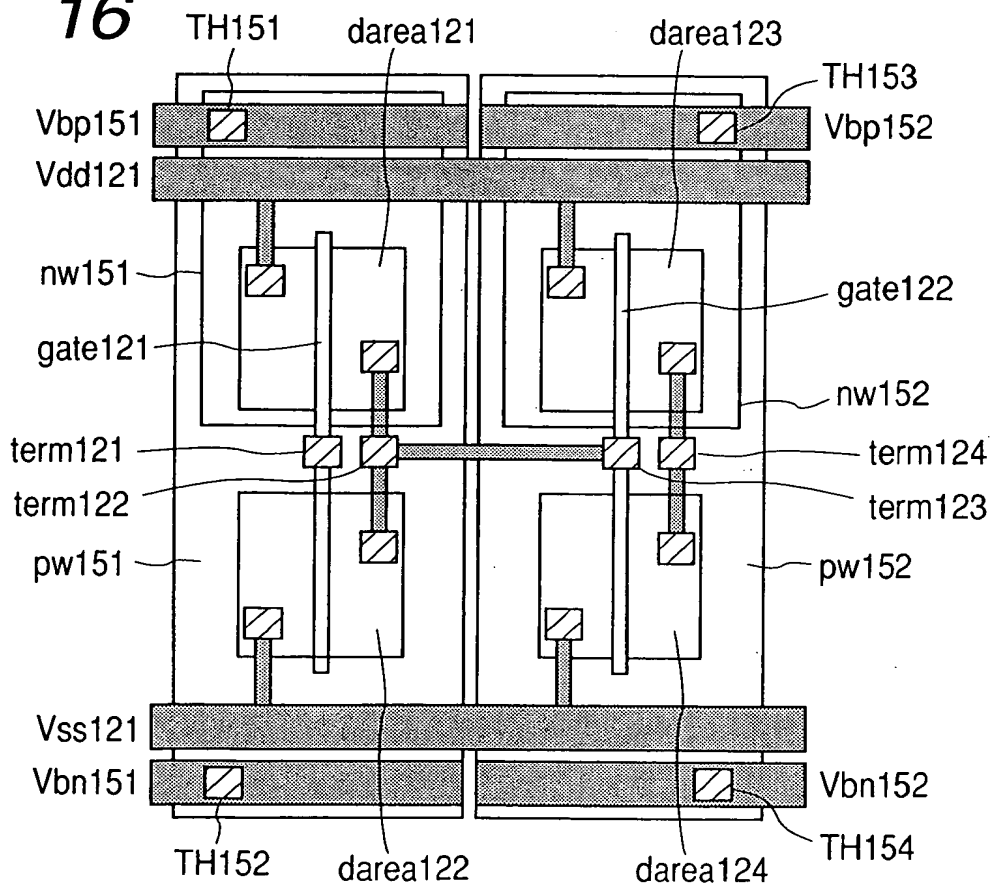
FIG. 15**FIG. 16**

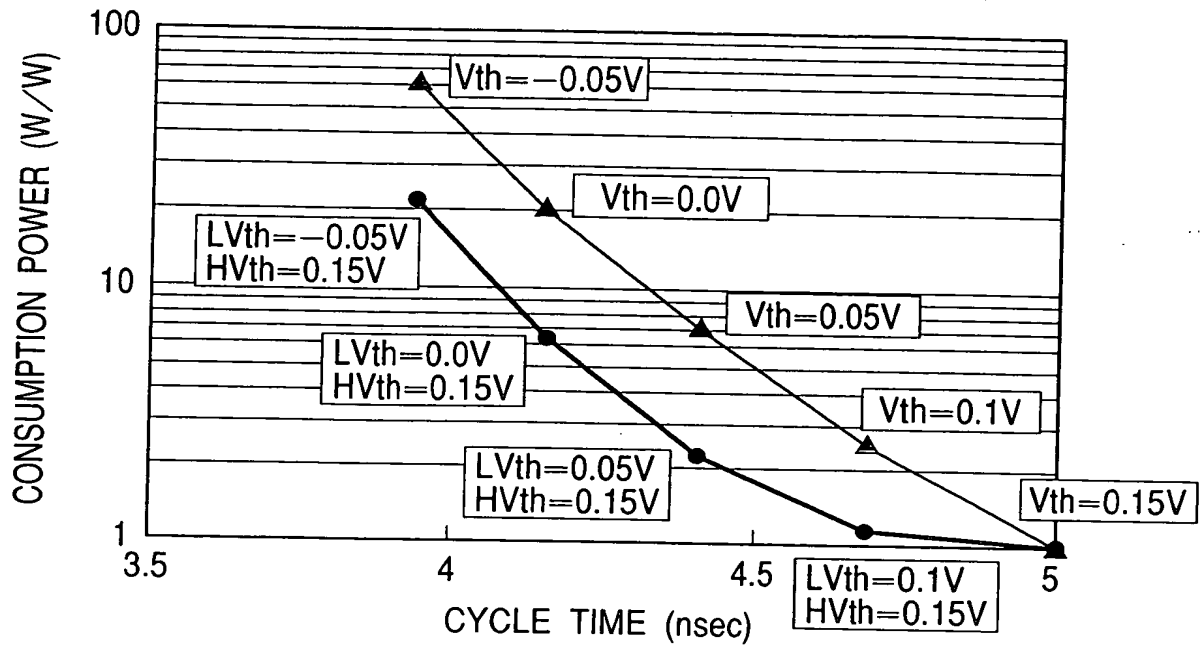
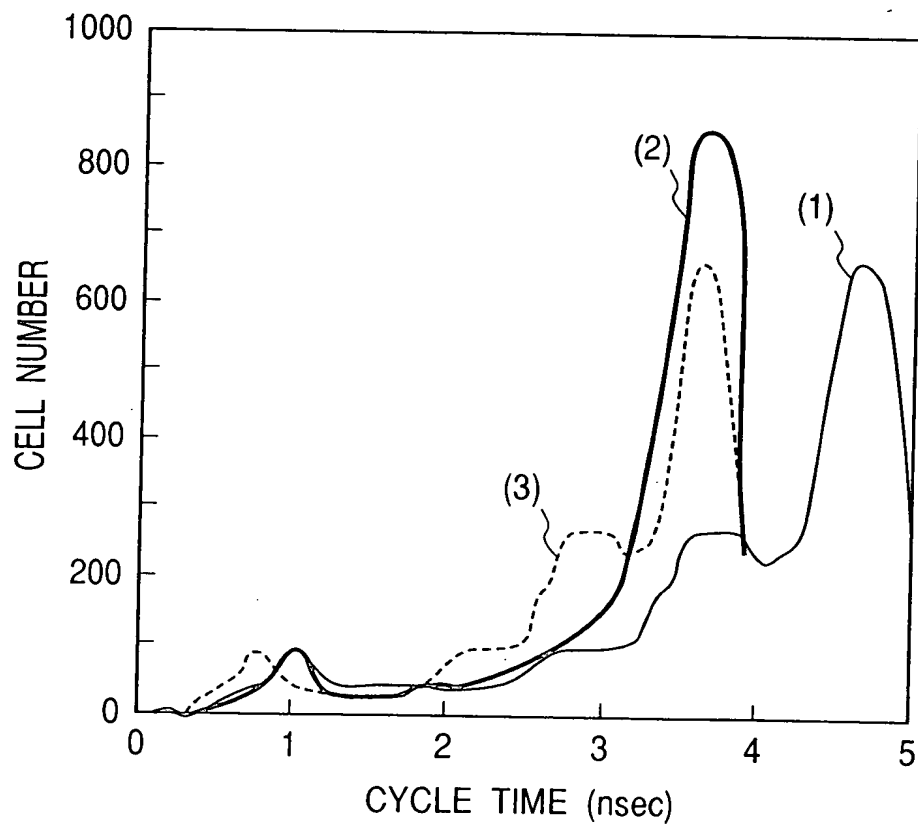
FIG. 17**FIG. 18**

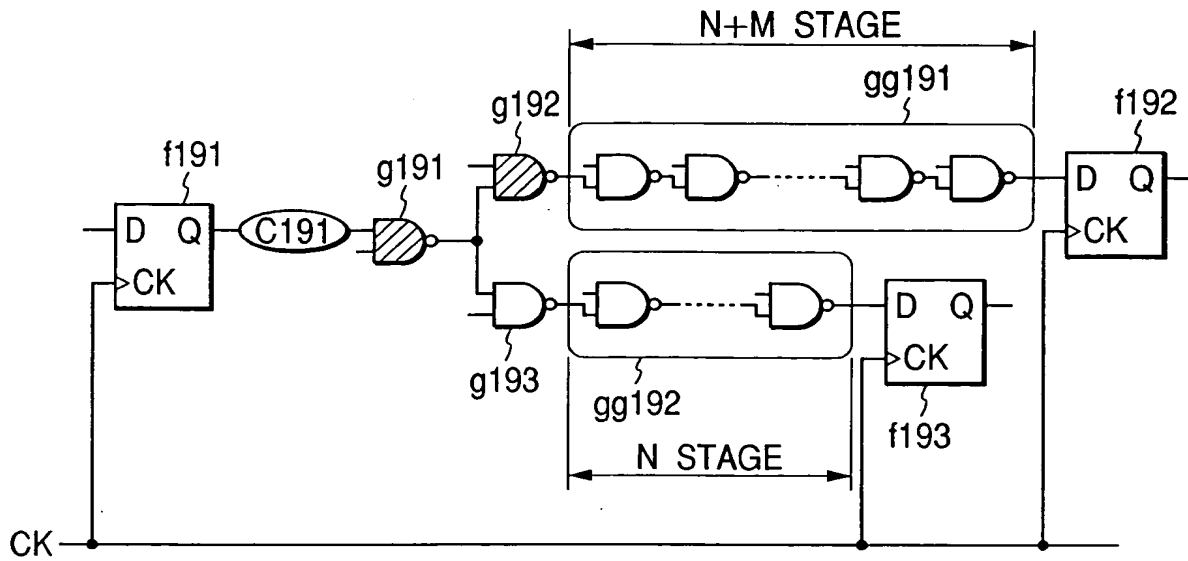
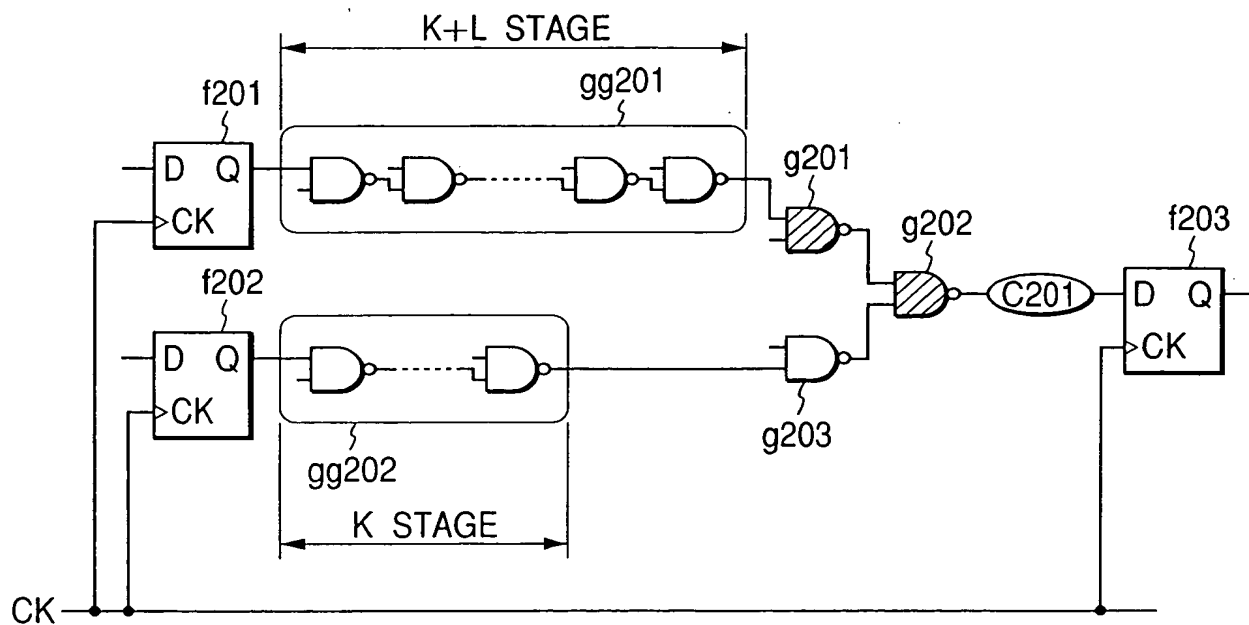
FIG. 19**FIG. 20**

FIG. 22

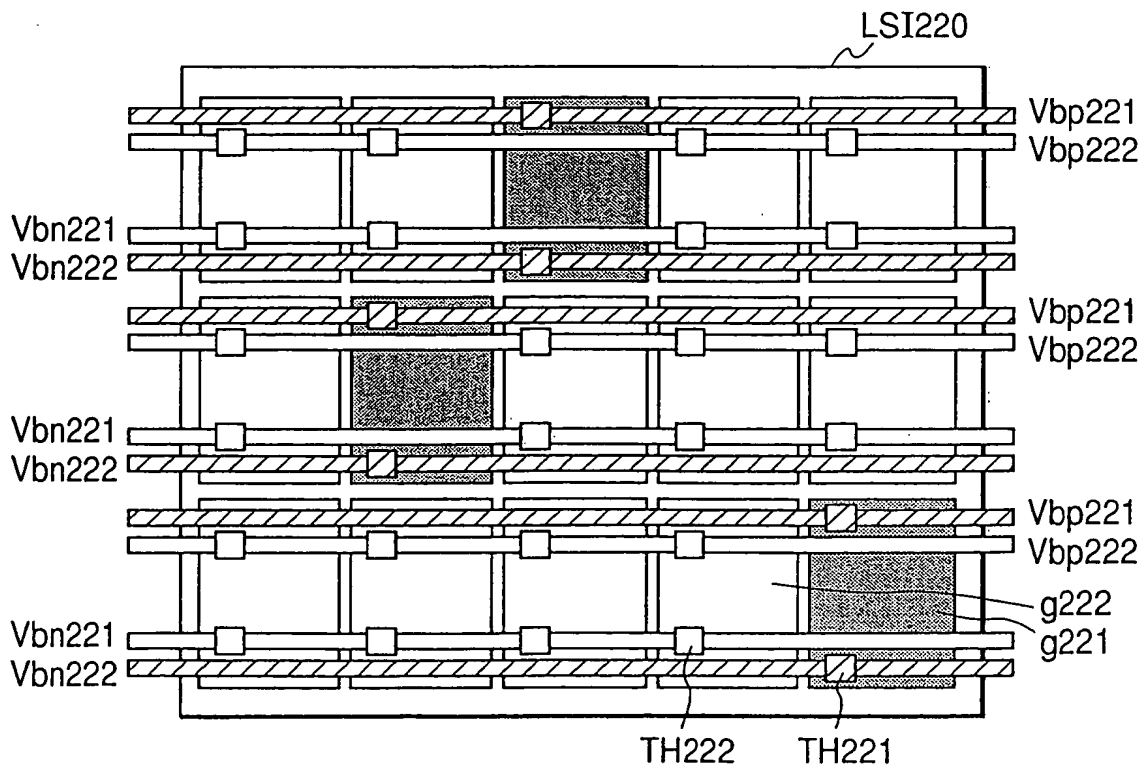


FIG. 23

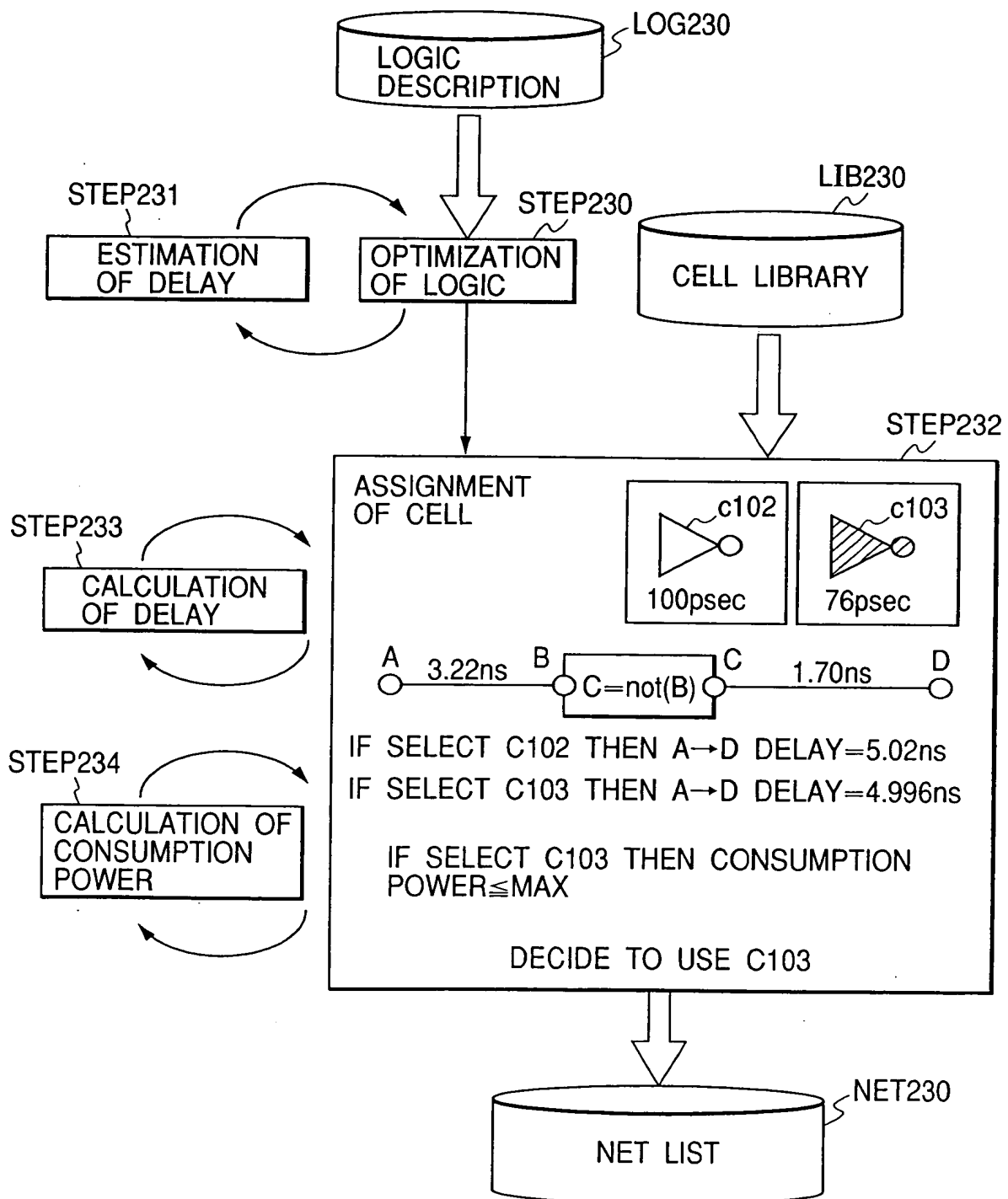


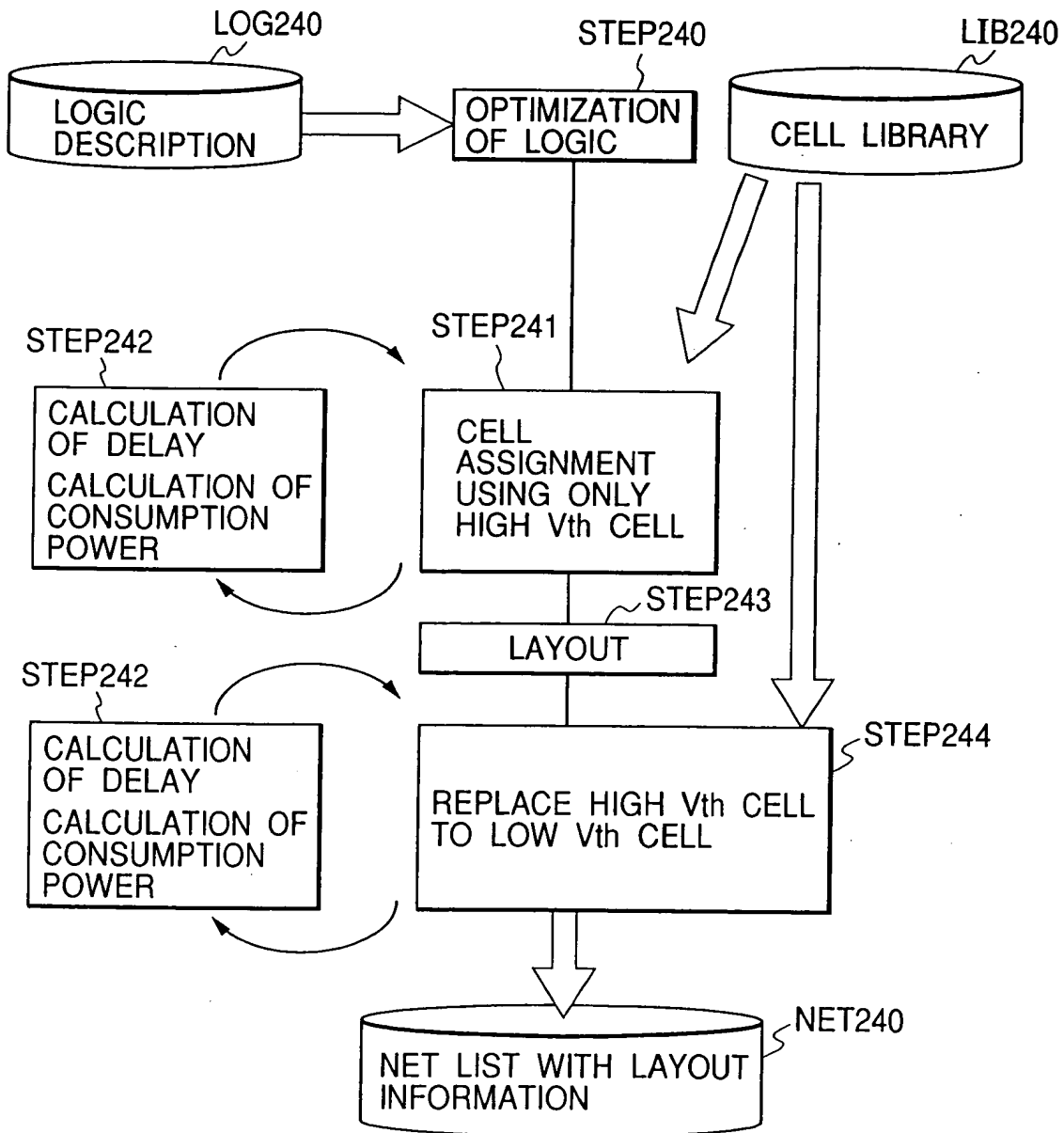
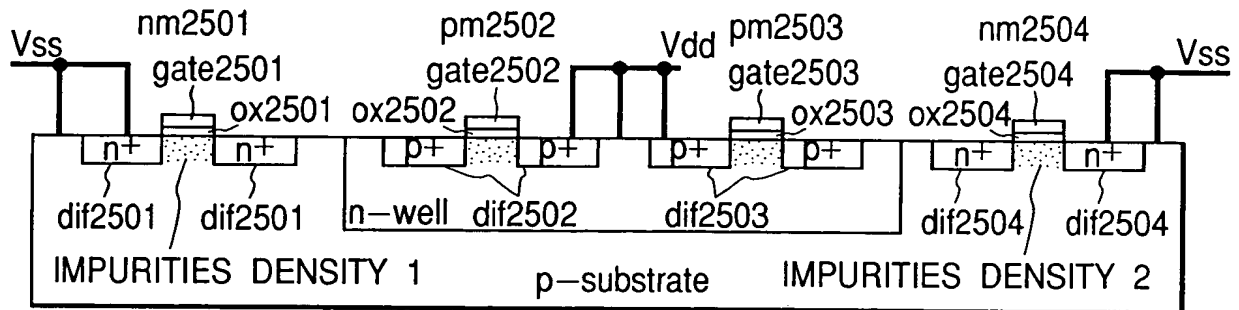
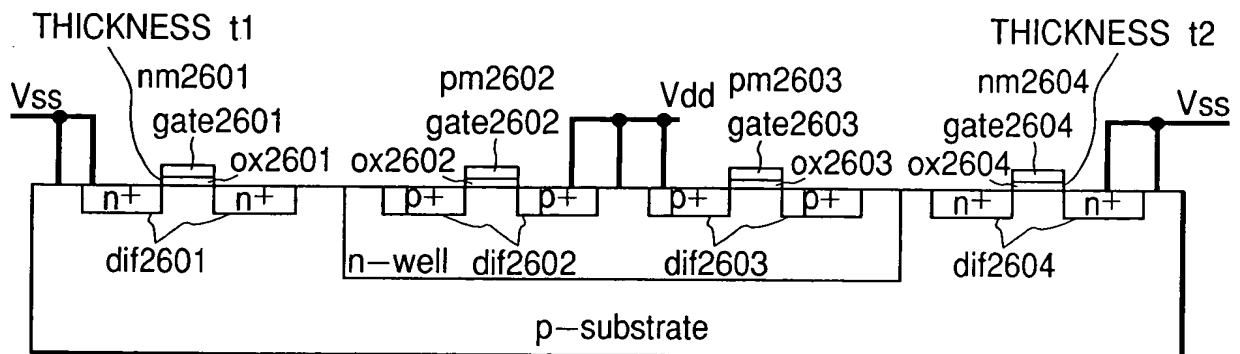
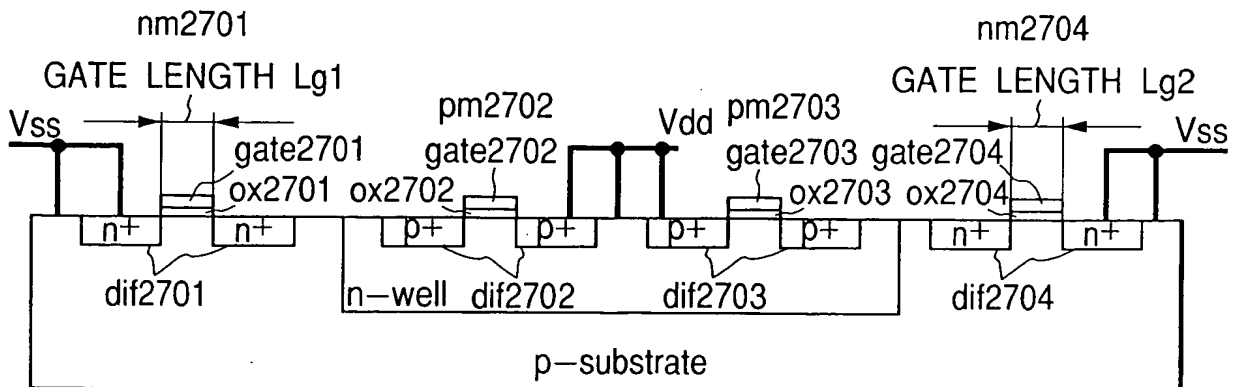
FIG. 24

FIG. 25**FIG. 26****FIG. 27**

The diagram illustrates the distribution of 16 DMA channels across various system components. Each component is represented by a grid of squares, where shaded squares indicate allocated channels.

- FPU:** A 7x5 grid (35 squares) with 16 shaded squares.
- BSC:** A 3x10 grid (30 squares) with 16 shaded squares.
- CASH:** A 3x10 grid (30 squares) with 16 shaded squares.
- CPU:** A 4x10 grid (40 squares) with 16 shaded squares.
- DMAC:** A 3x4 grid (12 squares) with 4 shaded squares.
- INT:** A 2x5 grid (10 squares) with 8 shaded squares.
- CPG:** A 2x4 grid (8 squares) with 8 shaded squares.